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Paper Code: MTMC012	Roll No.									

M. TECH.
FIRST SEMESTER THEORY EXAMINATION, 2016-2017
DESIGNING WITH ASICS

Time: 3Hours *Max. Mark: 70*

Note- ***Attempt All Questions. All Questions carry equal marks*:-**

1. **Attempt any FOUR of the following questions:**
   (a) Differentiate between Full Custom and Semi Custom ASICS.
   (b) Explain the various stages of ASIC design flow.
   (c) Describe the various parameters considered for ASICS variable cost. What is the most critical parameter and why?
   (d) What are the basic features that an ASIC cell library should satisfy? Explain in brief.
   (e) Explain the various models to withstand EOS and discuss the problem EOS.
   (f) Discuss the different type of assembly tools.
2. **Attempt any FOUR of the following questions:**
   (a) Explain the working of a CMOS inverter in detail with respect to its transfer characteristics.
   (b) Discuss all the types of Transistor Parasitic Capacitance.
   (c) Explain XILINX FPGA design flow.
   (d) Comment on Optimum delay and Optimum number of cells.
   (e) Define the term logic synthesis. How we will use logic synthesis in designing of FPGAs?
   (f) How do transistor resistance, parasitic capacitance and load capacitance affect the logic cell delay in ASICs? Explain.
3. **Attempt any TWO of the following questions:**
   (a) Enlist different types of Low Level Design Languages. Explain with an example.
   (b) Explain the various steps involved in the schematic design entry for ASICs.
   (c) Write the VHDL code for:
      (i) positive edge-triggered D flip-flop (ii) sequence detector
4. **Attempt any TWO of the following questions:**
   (a) What are the advantages of Verilog HDL over VHDL? What is the difference between structural and behavioural data flow modeling in Verilog?

(b) Define EDIF and explain the hierarchical nature of an EDIF file.

(c) Discuss the various logic cell models.

5. Attempt any TWO of the following questions:

(a) What are the goals of Placement in microelectronics? Explain any two placement algorithms.

(b) Explain the process of channel allocation in floor planning and what is cyclic constraint in this?

(c) What are the challenges in routing? Explain Global Routing.