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Paper Code: **MTMC-101**	**Roll No.**									

M. Tech.
FIRST SEMESTER EXAMINATION, 2016-17

ANALOG CMOS DESIGN

[Time: 3 Hours] [Max. Marks: 100]

Note: Attempt all questions. All question carry equal marks

1. Attempt any two parts of the following: - **(10x2=20)**

(a) Determine the small signal gain and the input common mode range (CMR) for the diff-amps shown in Fig 1. Estimate the slew-rate limitations in charging and discharging a 2pF capacitors tied to the outputs of the differential-amps as shown in figure 1

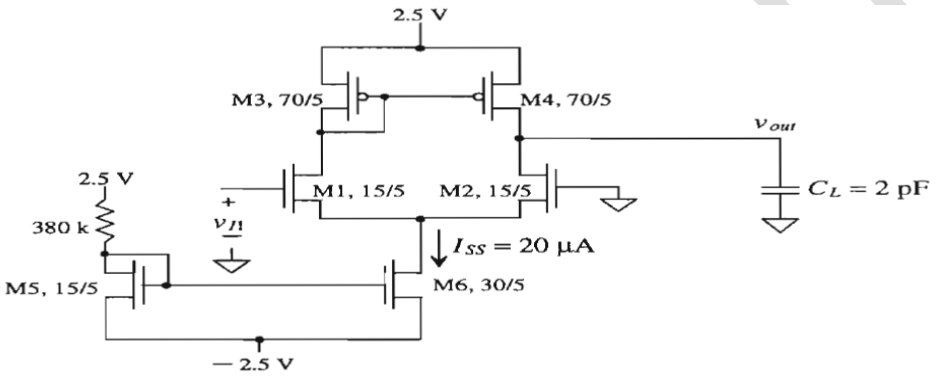

Figure1

(b) Draw a CMOS Op-Amp circuit. Discuss design parameters with characteristic. Explain the circuit analysis on the basic of the following design Parameter (i) Differential Amplifier Bias Current Iss (ii) Selection of the Second stage bias current.

(c) Draw and analyze the source cross- coupled differential amplifier using MOSFETs. If I_{ss}=10 μA and all nMOS have a (15/5) size while all pMOS have a (70/5) size, estimate the maximum difference in potential between the two inputs. Why does this pair not exhibit slew rate limitations?

2. Attempt any four parts of the following:- **(5x4=20)**

(a) Derive the expressions for the peak current deviation and the times it takes the output current to return to its steady value for simple current mirror (current sink) V_{DD}= -Vss=2.5V and C_{gd2}=5.7fF,C_{gs1}=C_{gs2}=40fF. If the step rises very quickly then determine ΔVGS.

(b) Develop a band gap voltage reference circuit and determine the following: (i) Vref (ii) The conditions under which the TC of the reference is zero.

(c) Design a 3V reference using the MOSFET only voltage divider assuming VDD= 5V and Vss =0V. Determine the temperature coefficient of the reference. Compare the power dissipation when L_1=L_2=5 μm, V_{Thn} =0.83 V, V_{Thp} = 0.91V, K_{pn}= 50 μA/V^2 and K_{pp}=17 μA/V^2.

(d) Design three current sources with values of 10, 20 and 50μA using n-channel current sink of 10μA. Assume V_{DD}= -Vss=2.5V, V_{GS}= 1.2 V and length of the devices= 5 μA, V_{Thn}= 0.83 V, V_{Thp} = 0.91V, K_pn= 50 μA/V^2 and Kpp=17 μA/V^2

(e) Write a short notes on Switch Capacitor Integrator.

(f) Design a Double Cascode current sink using VDD= -Vss=2.5V to sink a current of 10μA and determine the output resistance also

3. Attempt any *two* parts of the following:- **(10x2=20)**

(a) Draw the CMOS configuration of Operational Transconductance Amplifier and discuss its advantages and limitations.
(b) Design a universal biquad gm-C filter using two identical OTA and determine natural frequency and Q of the filter. Enlist the transfer function for each (i.e LP, HP, BP, BR) configuration.
(c) Determine the gain and bandwidth of the amplifier as shown in figure 2
C_{db1}=5.5fF C_{gd1}=1.9fF C'_{ox}=800aF/μm^2

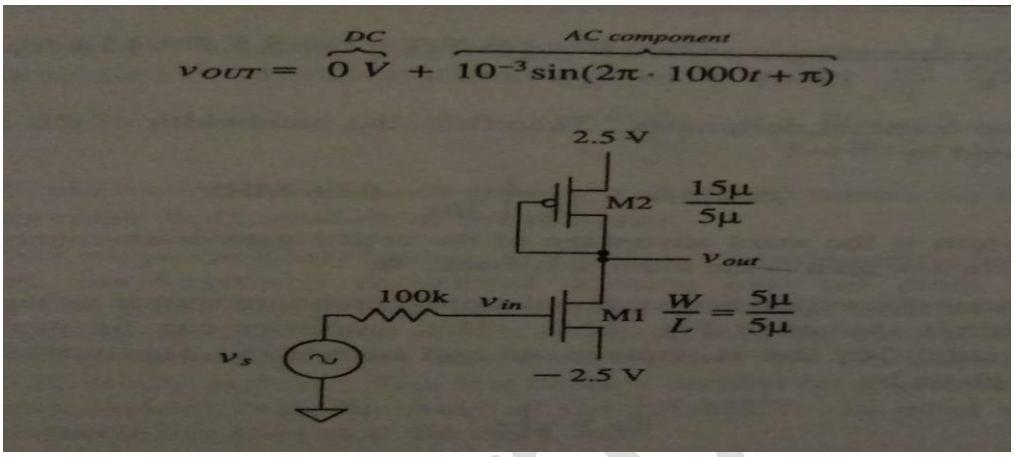

Figure 2

4. Attempt any *four* parts of the following:- **(5x4=20)**

(a) A DAC has a full–scale voltage of 4.97 using a 5V reference, and its minimum output voltage is limited by the value of one LSB. Determine the resolution and dynamic range of the converter.
(b) Design a 3-bit charge scaling DAC and find the value of the output voltage for $D_2D_1D_0$ =010. Assume that V_{REF} =5V and C=0.5pF
(c) Draw a block diagram of a Flash ADC and discuss its advantages and limitation
(d) Perform the operation of a 3-bit successive approximation ADC with VREF = 8. Make a table that consists of $D_2D_1D_0$, B_2 B_1 B_0, V_{OUT} and the comparator output, which shows the binary search algorithm of the converter for V_{IN}=5.5 V and 2.5V.
(e) Draw a small signal model and discuss the frequency response of common source amplifier with active load.
(f) Design a 3 bit DAC using a R-2R architecture with R=1kΩ, R_F=2kΩ and V_{REF}=5V. Assume that the resistance of the switches are negligible.

5. Attempt any *four* parts of the following: - **(5x4=20)**

(a) Analog CMOS Multiplier
(b) CMOS Comparator
(c) Develop a CMOS Wilson current mirror with small signal model circuit and determine the output resistance.
(d) β multiplier reference self biasing circuit.
(e) Sensitivity and Temperature Analysis for simple current mirror (Current Sink) circuit.
(f) Draw a circuit for Cascode differential amplifier and determine the common mode range