Paper Code: EC-703/EEC-703	**Roll No.**									

B.Tech.
SEVENTH SEMESTER EXAMINATION, 2016-17
VLSI DESIGN

[Time: 3 Hours] [Max. Marks:100]

Note: Attempt all questions. All questions carry equal marks

1. Attempt any four parts of the following**:-** **(5x4=20)**

(a) Explain the CMOS Inverter circuit operation with the help of VTC, clearly mark the operating regions of nMOS and pMOS transistors on it. Also calculate expression of switching voltage (V_{th}) for the same. Using the expression for switching voltage (V_{th}) find out the relation between (W/L)n and (W/L)p for an ideal symmetric inverter.
(b) Define the VLSI design process and draw Y- Chart.
(c) Define the layout design rules by defining micron for any particular technology. Draw a stick diagram of CMOS NOR gate
(d) Explain the terms Regularity, Modularity, Locality and Design Hierarchy. Define all types of MOSFET capacitances
(e) Explain Scaling, Narrow Channel effect and Channel Length Modulation in MOS.
(f) Discuss the classification of Dynamic CMOS logic families.

2. Attempt any two parts of the following**:-** **(10x2=20)**

(a) Consider a CMOS inverter circuits with the following parameters V_{DD} = 3.3V, V_{Ton} = 0.6V, V_{Top}= -0.7V, k_n = 200µA/V^2, k_p= 80µA/V^2, k_R = 2.5 Calculate the noise margin of the circuits.

(b) Consider a CMOS inverter, with the following device parameters, V_{DD} = 3.V, V_{Ton} = 0.6V, V_{Top} = -0.7V , $\mu_n C_{ox}$ = 60µA/V^2, $\mu_p C_{ox}$ = 20µA/V^2, λ= 0. Determine the $\left(\frac{W}{L}\right)$ rations of the nMOS and the pMOS transistors such that the switching threshold is V_{th} = 1.5V.

(c) Design the circuit described by the Boolean function $Y = \overline{(A+C)(B+C)(D+E)}$ using CMOS logic. Calculate the equivalent CMOS inverter circuit for simultaneous switching of all inputs assuming that $\left(\frac{W}{L}\right) = 10$ for pMOS transistor and $\left(\frac{W}{L}\right) = 5$ for all nMOS transistor.

3. Attempt any two parts of the following**:-** **(10x2=20)**

(a) Explain the CMOS inverter switching characteristic using the digital model. Explain the definitions of delays and transition times. Prove that for a CMOS inverter switching voltage

$$V_{th} = \frac{V_{To,n} + (V_{DD} + V_{To,p})\sqrt{\frac{1}{K_R}}}{1 + \sqrt{\frac{1}{K_R}}}$$

(b) Estimate the intrinsic propagation delay $t_{PHL}+t_{PLH}$ of a three-input NAND logic gate using minimum size transistor (R_n=8kΩ, Rp=24kΩ and C_{outn} =4.8fF).Estimate the circuit delay also when the gate is driving a load capacitance of 100fF.

(c) Discuss the operation of five stage Ring Oscillator circuits & determine the oscillation frequency with PDP (R_n=8kΩ, R_p=24kΩ, C_{outn} =4.8fF, V_{DD} =5V).

4. Attempt any four parts of the following**:-** **(5x4=20)**

(a) Design 2 input EXOR logic gate using CMOS transmission gate.

(b) Explain the behavior of pass transistor in dynamic CMOS logic implementation with considering the transfer of logic 1 and 0 by NMOS.

(c) In a CMOS inverter power supply V_{DD} =5V, determine the fall time, which is define as the time elapsed between the time point at which $V_{out}=V_{90\%}$=4.5V and the time point at which $V_{out}=V_{10\%}$ =0.5. The output load capacitance is 1pF. The nMOS transistor parameters are as follows: V_{Tn}=1.0V, $\mu_n C_{ox}$ = 20μA/V^2, $\left(\frac{W}{L}\right)_n = 10$.

(d) Design a D flip-flop using CMOS logic circuits.

(e) In a logic Design logic function is $Z = \overline{(A+B+C+D)(E+F+G)(H+I)}$ implemented with inputs (A,E,H) are high and other inputs are low. Draw a domino CMOS circuits diagram with implements Z.

(f) Draw a neat diagram of CMOS SRAM cell and explain it.

5. Attempt any four parts of the following**:-** **(5x4=20)**

(a) Define the term Controllability and Observability. Discuss in brief Ad-hoc Testable design techniques.

(b) Define different types of defects and faults. Explain the implementation of Built-In Self Test (BIST) design techniques for VLSI circuit testing.

(c) What are the various source of power dissipation in CMOS circuit with proper diagram?

(d) Discuss the variable threshold CMOS and multi threshold CMOS circuit for low power VLSI Design.

(e) Define the process of estimation and Optimization of switching activity with an example.

(f) Discuss the operation of DRAM cell with suitable CMOS circuits.