Paper Code: EC-309	**Roll No.**									

B. TECH.
THIRD SEMESTER EXAMINATION, 2016-17
DIGITAL LOGIC DESIGN

[Time: 3 hrs.] [Max. Marks: 100]

Note:- Attempt All questions. All questions carry equal marks.

1. Attempt any *four* parts of the following: - **[5x4=20]**

(a) Perform the arithmetic operations (+42) + (-13) and (-42) – (-13) in binary using the signed-2's complement representation for negative numbers.
(b) Simplify the following function with Karnaugh-map (K-map) and implement using NOR gates only: $F(x, y, z) = \sum m\ (0, 2, 6)$.
(c) Simplify the following function and implement with two-level NAND gate circuit:
F (A, B, C, D) = BD + BC$\overline{D}$ + A$\overline{B}\,\overline{C}\,\overline{D}$
(d) Simplify the following Boolean function in (a) sum of products and (b) product of sums: $F\ (A, B, C, D) = \sum m\ (0, 1, 2, 5, 8, 9, 10)$
(e) Find the minterms of the following Boolean expressions by first plotting each function in a map: $F\ (w, x, y, z) = wxy + \bar{x}\,\bar{z} + \bar{w}xz$
(f) Simplify the following Boolean function using the tabulation method:
$F\ (A, B, C, D) = \sum m\ (0, 1, 2, 8, 10, 11, 14, 15)$

2. Attempt any *four* parts of the following: - **[5x4=20]**

(a) Design an 8-bit parallel binary adder to add A and B.
Where A = 10110101, B = 11001101. (Show with proper labeling)
(b) Implement a full subtractor using 3 to 8 line decoder.
(c) Design a BCD adder to add $(20)_{10}$ and $(12)_{10}$.
(d) Design a BCD to excess-3 code converter using various logic gates.
(e) Design a 4-bit binary magnitude comparator showing output y=1 when both numbers A and B are equal and y=0 otherwise.
(f) Implement a full adder using 4x1 multiplexers.

3. Attempt any *two* parts of the following: - **[10x2=20]**

(a) (i) Design 4-bit switch-tail ring counter using D flip-flops.
(ii) Design Mod-6 gray code counter using J-K flip-flops.

(b) Draw and explain 4-bit Parallel In Serial Out (PISO) shift left register using D flip-flops.

(c) Draw the BCD ripple counter. Also explain with timing diagram.

4. Attempt any *two* parts of the following: - **[10x2=20]**

(a) Explain race-around condition in detail. Give the remedy to remove it using gate level diagram.

(b) Design a sequential circuit having three flip-flops A, B and C, one input, x and one output y for the following state diagram (fig.1). The circuit is to be designed by treating the unused states as don't-care conditions. (Use D flip-flops in the design)

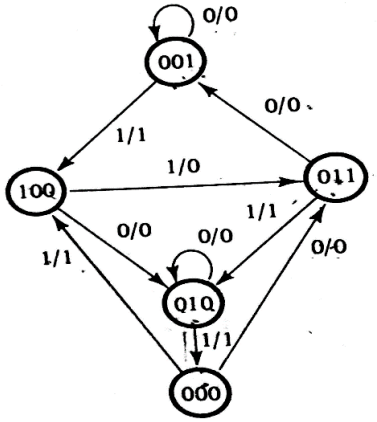

Fig.1

(c) Perform the state reduction for the given state diagram (fig.2) by deriving its state table. Also draw the reduced state diagram.

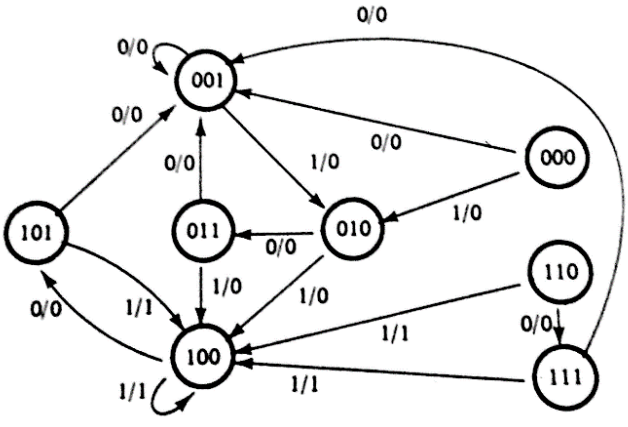

Fig.2

5. Attempt any *two* parts of the following: - **[10x2=20]**

(a) Explain hazards in detail. Find a circuit that has no static hazards and implement the Boolean function: $F(A,B,C,D) = \sum m(0,2,6,7,8,10,12)$

(b) Design a combinational circuit using a ROM. The circuit accepts a 3-bit number and generates an output binary number equal to the square of the input number.

(c) A combinational circuit is defined by the functions

$F_1(A, B, C) = \sum m(3, 5, 6, 7)$

$F_2(A, B, C) = \sum m(0, 2, 4, 6)$

Implement the circuit with PLA, PAL and PROM.