Paper Code: EC302 **Roll No.** | | | | | | | | | | |

B.TECH
(SEM III) ODD SEMESTER EXAMINATION 2016-17
SWITCHING THEORY AND LOGIC DESIGN

[Time: 2 hrs.] **[Max. Marks: 50]**

Note- ***Attempt All Questions. All questions carry equal marks:-***

1. Attempt any FOUR questions of the following:- **(3.5 X 4 = 14)**

(a) Simplify the following expression using K-map:

$$F(A, B, C, D) = A.B(C \oplus D) + \overline{A}.B(C \odot D) + C.D(A \odot B) + \overline{C}.D(A \oplus B)$$

(b) Design a BCD to Excess-3 converter.

(c) Implement the following function with a multiplexer using A, B, C variables to the select lines: $F(A, B, C, D)=\Sigma m(0, 1, 3, 4, 8, 9, 15)$.

(d) Convert the RS flip flop to JK flip flop showing all the steps of conversion.

(e) Design a 4-Bit magnitude comparator.

(f) Find the minimal SOP for the following Boolean expression using Quine-Mc-Cluskey method.

$$F(A, B, C, D) = \Sigma\, m(1, 2, 3, 7, 8, 9, 10, 11, 14, 15)$$

2. Attempt any TWO questions of the following: **(6 X 2 = 12)**

(a) By means of a timing diagram show the signals of the outputs X, Y and Z in Fig. 1, as a function of the two inputs A and B for all combinations. If the propagation delay of one gate is 5μs then, what will be the propagation delay of output Z?

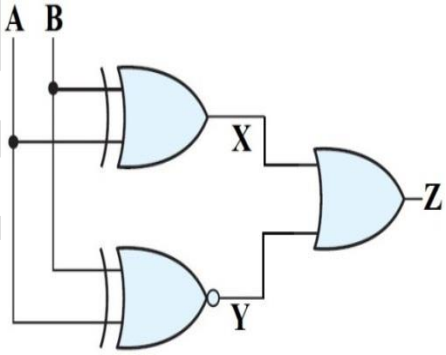

Fig.1

(b) Design a 3 bit up/down ripple counter.

(c) Design a combinational circuit using a ROM that accepts a 3-bit number and generates an output binary number equal to the square of the input number.

(d) Design a combinational circuit that converts a 3-bit Gray code to a 3-bit binary number. Implement the circuit with (i) Ex-OR gate (ii) NAND gate only.

3. Attempt any THREE questions of the following: **(4x3 = 12)**

(a) Distinguish the difference between Mealy and Moore models. Explain with a relevant example. Identify the type of circuit is shown in Fig. 2? Draw state diagram of this.

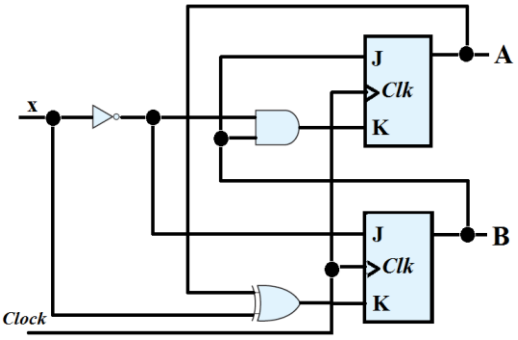

Fig.2

(b) Define Hazards? Explain different types of Hazards with proper example. Also discuss the methods by which it can be removed.

(c) Implement a Universal shift register with suitable diagram.

(d) Describe the basic properties of 4-bit Ring counter and Johnson counter.

4. **Attempt any TWO questions of the following:** **(6 X 2 = 12)**

(a) Implement the following function in PLA

$F_1(A,B,C) = \sum(0,1,2,4)$

$F_2(A,B,C) = \sum(0,5.6,7)$

(b) Reduce the state diagram shown in the Figure 3 and assign state using one shot scheme. What are the advantages of one hot scheme over general binary assignment?

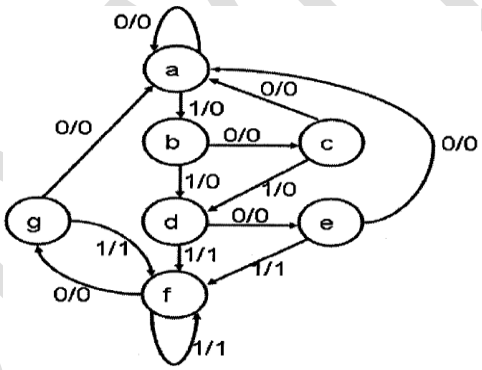

Fig.3

(c) Design a synchronous counter which repeats the following binary equivalent sequence of decimal numbers- 0, 2, 4, 6.

(d) For the following state diagram obtain the state table, input equation, output equation and design the logic diagram using J-K flip-flop.

(e)