Roll No.										

Paper Code: CS-505

B. TECH.
FIFTH SEMESTER EXAMINATION, 2016-2017
COMPUTER ARCHITECTURE

[Time: 2 Hours] [Total Marks: 50]

Note: Attempt *ALL* questions. Assume suitable data, if required. All question carry equal marks.

1. Attempt any four Questions [4 x 2.5=10]

(a) A computer has 32 bit instruction and 8 bit addresses. If there are **250 three address** instructions and **1024 two address** instruction, then how many **one address instructions** can be formulated?

(b) Consider virtual memory environment in which main memory access time is **10 µs** and TLB hit ratio is **0.8**.If Effective Access Time is **13µs** then calculate **TLB lookup** time.

(c) What is the **BUS arbitration**? Why is it needed?

(d) An 8 bit register contains the binary value 11101101.What is the register value after **circular shift left and right**?

(e) What are the various phases for executing an instruction?

(f) What is the difference between **SRAM** and **DRAM**?

2. Attempt any two questions of the following:- **[5 x2=10]**

(a) A relative mode branch type of instruction is stored in memory at an address equivalent to decimal 750. The branch is made to an address equivalent to decimal 500.

(i) What should be the value of the relative address field of the instruction (in decimal)?

(ii) Determine the relative address value in binary using 12 bits. (Why must the number be in 2's complement?)

(iii) Determine the binary value in PC after fetch phase and calculate the binary value of 500. Then show that the binary value in PC plus the relative address calculated in part (ii.) is equal to the binary value of 500.

(b) An 8 bit CPU has the register R input to 2's complement ALU. The current value of R is the $(E7)_{16}$. For each of the following instructions determine the content of the status register having bits V, S, C (V=Overflow, S=Sign, C=Carry) and interconnected to the ALU.

(i) ADD immediate operand $(BD)_{16}$ to R.

(ii) SUB immediate operand $(68)_{16}$ from R.

(c) State Booth's algorithm for multiplication of two numbers.

3. Attempt any two questions of the following:- **[5 x2=10]**

(a) Write control sequence for the execution of following instruction **followed by an interrupt.** Assume that the address of interrupt service routine is stored at memory location ***M***.

(Assume the processors which have the general purpose register R0, R1, R2 and temporary register X, Y, Z special purpose register MAR, MDR, PC, IR, SP etc…)

SUB (R2+), (R1)

[(R2+1) ← (R2) - R1 Here, R1 contain numeric value. R2 contain the address of memory location. This instruction subtracts content of register R1 from the content of memory location pointed by register R2. And result is stored at memory location (R2+1)]

(b) Describe the principle of designing instruction set of a processor. Explain the important fields of instruction format.

(c) What is the difference between hardwired control and micro programmed control? What are the advantages and disadvantages in each control?

4. Attempt any two questions of the following:- **[5 x2=10]**

(a) A cache memory unit with a capacity of 512 MB is built using a block size of 128 KB. The size of the physical address space is 4 GB. If it uses **K-way set associative** mapping and **10 bit** is used for the **SETfield** then find the value of **K**. How many bits are needed to represent **TAG and WORD** fields for the **K-way set associative** mapping cache? If 3 extra bits are used per TAG to show the status of cache blockthen what is the minimum size of **TAG directory** in Bytes?(1 Word = 1 Byte).

(b) In a virtual memory system, length of virtual address is 40 bit, **page size** is 4 MB and **page table size** is 2^{19}Byte. (Assume that no protectionbit is used in Page table). What is the **size ofphysical address space?** If it implements 128 entries associative TLB then what is the **size of TLB?**

(c) What do you understand by level of memory hierarchy? Discuss various design considerations of memory hierarchy?

5. Attempt any two questions of the following:- **[5 x2=10]**

(a) What are the basic differences between interrupt initiated I/O and programmed I/O? Explain in detail.

(b) Discuss the DMA data transfer with the help of block diagram.

(c) How many characters per second can be transmitted over a **2400-baud** line in each of the following modes? (Assume a character code of **sixteen bits.**)

(i.) Synchronous serial transmission

(ii.) Asynchronous serial transmission with two stop bits.

(iii.) Asynchronous serial transmission with one stop bits.