Paper Code: CS-505	**Roll No.**
Paper ID:	

B. Tech.
(SEM V) ODD SEMESTER EXAMINATION 2015-16
Computer Architecture

[Time: 2 hrs.] **[Max. Marks: 50]**

Q1. Attempt any four Questions ***[4 X 2.5]***

a.) A machine has a 32-bit architecture, with 1-word long instructions. It has 32 registers, each of which is 32 bits long and it can access 128 word physical addresses. It needs to support 50 instructions, which have an immediate operand, one Memory operand and one register operand. Assuming that the immediate operand is an unsigned integer, find the maximum value of immediate operand in decimal.

b.) Cache memory access time is **5ns** and Main memory access time is **20ns**. Suppose 90% of the memory accesses are found in the cache. Then calculate the **Average Memory Access** time.(Consider hit ratio for the main memory is 1)

c.) What is the difference between **Indexed Addressing** mode and **Base register addressing** mode?

d.) An 8 bit register contains the binary value 01100101.What is the register value after **arithmetic shift left and right**? And also indicate whether there is an **overflow?**

e.) What is the difference between **Interrupt** and **Exceptions?**

f.) What is the wrong with the following register transfer statements?

(i.) xT: PC ← MAR, PC← PC+1 (ii.) yT: R2←R1, R2←R3

Q2. Attempt any two Questions ***[2 X 5]***

a.) State Booth's algorithm for multiplication of two numbers.

b.) Design a digital circuit that performs the four logic operations of exclusive-OR, exclusive-NOR, NOR and NAND. Use two selection variables. Show the logic diagram of one typical stage.

c.) Following pair of numbers are given in signed 2's complement form. After performing addition operation on each pair of numbers what are the values of the **overflow (V), carry(C) and sign (S)** flags. (Register size of ALU is 8 bit).

(i) 10110101, 10011100 (ii) 11100111, 01001101

Q3. Attempt any two Questions ***[2 X 5]***

a.) Write the control sequence for the execution of the following instruction.

(Assume a single bus CPU consists of general purpose registers R0, R1, R2 temporary registers X, Y, Z and special purpose register MAR, MDR, PC, IR etc…)

SUB R_1, (R_2)

(On execution of above instruction, the memory operand whose address is in R_2 will be subtracted from the register R1 and result is stored in the register R_1)

b.) Discuss how address sequencing is carried out in micro-programmed control organization.

c.) Write difference between **Vertical and Horizontal** microprogramming?

Q4. Attempt any two Questions ***[2 X 5]***

a.) Discuss different types of RAM. How many 64M X 1 RAM chips are needed to provide a memory capacity of 4G-bytes?

b.) A cache memory unit with a capacity of 128MB is built using a block size of 64 KB. The size of the physical address space is 4 GB. Consider the word size is 1 Byte. How many bits are there in each of the **TAG, SET and WORD** fields for the **4-way set associative** mapping cache? If 2 extra bits are used per TAG to show the status of cache block. Then what is the minimum size of **TAG directory** in Bytes?

c.) In a virtual memory system, length of virtual address is 40 bit, size of physical memory is 8GB, and page size is 4 MB. (Assume that no protection bit is used in Page table). What is the **size of page table?** If it implements 128 entries TLB then what is the **size of TLB?**

Q5. Attempt any two Questions ***[2 X 5]***

a.) What is the main advantage of using interrupt initiated data transfer over transfer under program control without an interrupt?

b.) Describe strobe control, Handshaking for synchronous data transfer. What are advantages and disadvantages of both modes?

c.) How many characters per second can be transmitted over a 1200-baud line in each of the following modes? (Assume a character code of eight bits.)

(i.) Synchronous serial transmission

(ii.) Asynchronous serial transmission with two stop bits.

(iii.) Asynchronous serial transmission with one stop bits.