Paper Code: MEC-930 **Roll No.** | | | | | | | | | | |

M.Tech.
(SEM II) EVEN SEMESTER EXAMINATION, 2015-16
TESTING & VERIFICATION of VLSI CIRCUITS

[Time: 3 hrs.] **[Max. Marks: 100]**

Note- Attempt All Questions. All Questions carry equal marks.

Q.1. Attempt any **TWO** parts of the following. **[10x2=20]**

(a) What do you mean by testability of VLSI circuits? Why is verification of VLSI circuits required? Explain the testing mechanism.

(b) Explain the different kinds of physical faults that can occur in a CMOS chip, and relate to typical circuit failure.

(c) What is fault simulation? What are the different fault simulation techniques? Discuss each of them.

Q.2. Attempt any **TWO** parts of the following. **[10x2=20]**

(a) Explain the terms :

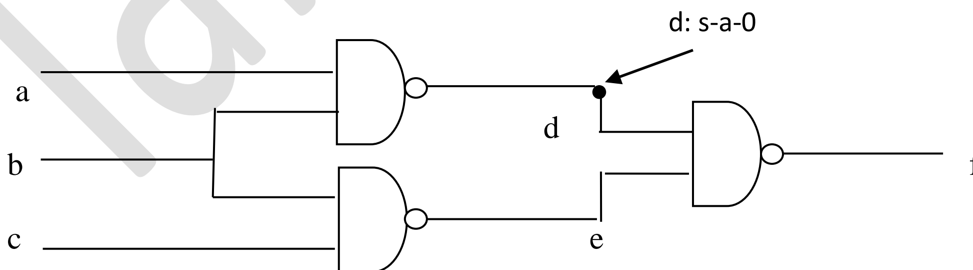
(i) Test and Testability (ii) System partitioning (iii) Test coverage (iv) Functionality tests.

(b) Discuss in detail the Bridging Fault Model and Delay Fault Model. Explain with suitable examples.

(c) Draw two inputs CMOS NAND gate. Find and explain what are the different possible single stuck at fault also compare the output for each case with fault free.. If a bridging exists between the source and drain at one of the driver transistor, find the conditions of input for average output.

Q.3. Attempt any **TWO** parts of the following. **[10x2=20]**

(a) Find the primitive D-Cube for two input NOR gate for output Z: s-a-1. Use D- algorithm to generate test vectors for d: s-a-0 in the circuit shown in figure.



(b) What do you mean by sensitized path? Describe the method of sensitized path based testing. Using sensitized path technique, find the test pattern to detect the fault d: s-a-0 and d: s-a-1 in the circuits shown in Figure.

(c) Explain Boolean difference method for test generation. Use Boolean difference method to generate test vectors for single stuck at fault at e: s-a-1 and e: s-a-0 faults in the circuit shown in Figure

Q.4. Attempt any **TWO** parts of the following. **[10x2=20]**

(a) What do you mean by DFT? Why is it needed? Explain with example, how controllability and observability of a circuit under test can be improved?

(b) How scan design techniques are used to test sequential circuit? Explain the working of the scan chain based technique with necessary circuit diagram.

(c) Draw the architecture of boundary scan test (BST) and explain the operation. Why is BST required?

Q.5. Write short notes on any **TWO** of the following. **[10x2=20]**

(a) Built-in Logic Block Observer (BILBO)

(b) Ad-hoc Testing

(c) Physical Verification

(d) Level Sensitive Scan Design (LSSD)

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