Roll No.										

Paper Code: MEC-908

M. Tech.
(SEM II) EVEN SEMESTER EXAMINATION, 2015-16
ADVANCED COMPUTER ARCHITECTURE

[Time: 3 hrs.] **[Max. Marks: 100]**

Note- Attempt All questions. All questions carry equal marks.

1. Attempt any ***two*** of the following questions:- **[10 x 2 = 20]**

   (a) Discuss the various computer architectures according to the Michael Flynn and system attributes Clock Rate and CPI, Performance Factors, and MIPS Rate.

   (b) What do you understand by shared-memory multiprocessor? Write a short note on UMA, NUMA, and COMA.

   (c) A 400 MHz processor was used to execute a benchmark program with the following instruction mix and clock cycle counts

Instruction type	Instruction count	Clock cycle count
Integer arithmetic	450000	1
Data transfer	320000	2
Floating point	150000	2
Control transfer	80000	2

   Determine the following:

   i. Effective CPI
   ii. MIPS Rate
   iii. Execution time

2. Attempt any **two** of the following questions:- **[10 x 2 = 20]**

   (a) Explain different types of static connection networks with parameter node degree, network diameter, number of links, and bisection band width.

   (b) Write short notes on dynamic connection networks and their types with diagram. Design a 16x16 Omega network using 2x2 switches and perfect shuffle.

   (c) Construct a 64-input Omega network using 4x4 switch modules in multiple stages. How many permutations can be implemented directly in a single pass through the network without blocking?

3. Attempt any ***two*** of the following questions: - **[10 x 2 = 20]**

(a) Define the following basics terms associated with memory hierarchy design:

i. Virtual address space.
ii. Physical address space.
iii. Address mapping.
iv. Cache blocks.
v. Page fault.

(b) Consider a cache (M_1) and memory (M_2) hierarchy with the following characteristics: M_1: 64K words, 5ns access time and M_2: 4M words, 40 ns access time Assume eight – word cache blocks and a set size of 256 words with set associative mapping.

(c) Construct a direct – mapping cache design where n = 16 blocks are mapped to m = 4 blocks frames, with four possible sources mapping into one destination using modulo-4 mapping.

4. Attempt any ***two*** of the following questions: - **[10 x 2 = 20]**

(a) What is pipelining explains with an example and formulates the speedup (S) for a pipeline processer?

(b) Consider the execution of a program of 15,00,000 instructions by a linear pipeline processor with a clock rate of 1000 MHz. Assume that the instruction pipeline has five stages and that one instruction is issued per clock cycle. The penalties due to branch instructions and out-of-sequence executions and ignored.

i. Calculate the speedup factor in using this pipeline to execute the program as compared with the use of an equivalent non pipelined processor with an equal amount of flow-through delay.
ii. What are the efficiency and throughput of this pipelined processor?

(c) A pipeline with four stages is characterized by the reservation table 1:

Table 1

	T1	T2	T3	T4	T5	T6
S1	X					X
S2		X		X		
S3			X			
S4				X	X	

i. Obtain initial collision vector.
ii. Draw state diagram and obtain MAL.
iii. What is the optimized MAL and upper bound on MAL.

5. Attempt any ***two*** of the following questions:- **[10 x 2 = 20]**

(a) Discuss the multiprocessor system interconnects and draw the figure of interconnection structures in a generalized multiprocessor system with local memory, private caches, shared memory, and shared peripherals.

(b) What is the hierarchal bus systems, explain the packaged of hierarchal bus systems at different levels with neat diagram.

(c) Explain the following:

(i) Crossbar Switch and Multiport Memory
(ii) *Multistage and Combining Networks*