Paper Code: MEC-907 **Roll No.** | | | | | | | | | | |

M. Tech.
(SEM. II) EVEN SEMESTER THEORY EXAMINATION, 2015-16
VLSI DESIGN

[Time: 3 hrs.] **[Max. Marks: 100]**

Note: Attempt all questions. All question carry equal marks.

Q.1. Write a short notes on any four of the following:- **[5x4=20]**

(a) Enlist the classification of CMOS digital logic families. Draw a 4X1 multiplexer using Transmission Gate (TG).
(b) Explain the CMOS inverter switching characteristic using the digital model and explain the definitions of delays and transition times.
(c) Discuss the operation of pass transistor in dynamic logic circuit
(d) Calculate the shift in the transfer characteristic for a CMOS inverter, when the βn/βp ratio is varied from 1/1 to 10/1.
(e) Design D flip-flop using TG CMOS circuits.
(f) Draw and explain the design flow diagram of VHDL in brief

Q.2. Attempt any two parts of the following:- **[10x2=20]**

a) Consider a CMOS inverter, with the following device parameters, V_{DD} = 3.V, V_{Ton} = 0.6V, V_{Top} = -0.7V , $\mu_n C_{ox}$ = 60μA/V^2, $\mu_p C_{ox}$= 20μA/V^2, λ= 0. Determine the $\left(\frac{W}{L}\right)$ rations of the nMOS and the pMOS transistors such that the switching threshold is V_{th} = 1.5V.

b) Design the circuit described by the Boolean function $Y = \overline{A.(B+C)(D+E)}$ using CMOS logic. Calculate the equivalent CMOS inverter circuit for simultaneous switching of all inputs assuming that $\left(\frac{W}{L}\right) = 5$ for pMOS transistor and $\left(\frac{W}{L}\right) = 2$ for all nMOS transistor.

c) Design a cascade of inverters circuit to drive a large capacitive load with minimum delay.

Q.3. Attempt any *two* parts of the following**:-** **[10x2=20]**

(a) Design a CMOS buffer to drive a 20 pF capacitive load from the inverter with the size of (9/3). The t_{pHL} + t_{pLH} should be less than 11nS. Calculate the number of stages (N), area factor (A) and total delay for this buffer. Assume C'ox = 800 aF/μm2, channel length = 2 μm, R'n = 12 kΩ/sq, R'p= 36kΩ/sq.

(b) Estimate the intrinsic propagation delay t_{pHL}+t_{pLH} of a three-input NAND gate using minimum size transistor (R_n=8kΩ, R_p=24kΩ and C_{outn} =4.8fF).Estimate the circuit delay also when the gate is driving a load capacitance of 100fF.

(c) Estimate the oscillation frequency and power delay product of a five stage Ring Oscillator from the inverter with size of $W_n = W_p = 10$ μm. Assuming $C'_{ox} = 800aF/\mu m^2$, channel length=2μm, sheet resistance of N & PMOS i.e. R'n=12 kΩ/sq, R'p= 36 kΩ/sq.

Q.4. Attempt any two parts of the following**:-** **[10x2=20]**

(a) Explain the overview of power consumption in CMOS logic circuits.Write short notes on low power design through voltage scaling CMOS VLSI designs techniques.

(b) Discuss the estimation and optimization of switching activity in CMOS digital integrated circuit.

(c) (i) Design an adiabatic 2 input AND/NAND gate and explain it.
(ii)Discuss the operation of CMOS SRAM cell circuit.
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Q. 5. Attempt any four parts of the following:- **[5x4=20]**

(a) Explain the VLSI physical design cycle with suitable example.
(b) Explain Floor-planning is backend VLSI process. How you can use the Genetic algorithm to floor planning problem?
(c) Discuss the classification of placement algorithms with suitable examples.
(d) For the set A={1,2,3,4} and B={5,6,7,8} does the KL algorithm generate optimum partitioning? What is the balanced partition of the circuit that has maximum value of cutest?
(e) What are the limitations of Lee Algorithm for large circuit design, explain in details.
(f) Discuss the goals and objective of routing. Classify the routing categories.

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