Paper Code: MEC937	Roll No.									

M. Tech.
(SEM I) ODD SEMESTER EXAMINATION 2015-16
DESIGNING WITH ASICS

[Time: 3 hrs.] **[Max. Marks: 100]**

Note- ***Attempt All Questions. All Questions carry equal marks*:-**

1. **Attempt any FOUR of the following questions:**
   (a) Differentiate between the standard cell based ASIC and full custom ASIC?
   (b) Define the term break-even volume.
   (c) What is difference between channeled and channel less gate array?
   (d) Write the design flow of an ASIC.
   (e) What are PLD devices? Explain.
   (f) Write a note on cell compilers.

2. **Attempt any FOUR of the following questions:**
   (a) Explain the working of a CMOS inverter in detail with respect to its transfer characteristics.
   (b) Discuss all the types of Transistor Parasitic Capacitance.
   (c) What do you understand by the term "Half Gate ASIC"?
   (d) Comment on Optimum delay and Optimum number of cells.
   (e) Define the term logic synthesis. How we will use logic synthesis in designing of FPGAs?
   (f) How do transistor resistance, parasitic capacitance and load capacitance affect the logic cell delay in ASICs? Explain.

3. **Attempt any TWO of the following questions:**
   (a) Explain the EDIF Standard and write out the EDIF for an inverter icon.
   (b) Explain the various steps involved in the schematic design entry for ASICs.
   (c) Write the VHDL code for:
      (i) positive edge-triggered Dflip-flop
      (ii) an 8-bit ripple-carry adder
      .

4. **Attempt any TWO of the following questions:**
   (a) What are the advantages of Verilog HDL over VHDL? What is the difference between structural and behavioral data flow modeling in Verilog?
   (b) Synthesize multiplexers and decoders in Verilog.
   (c) Discuss the various logic cell models.

5. **Attempt any TWO of the following questions:**
   (a) What is the goal of system partitioning in microelectronics? Explain any two partitioning algorithms.
   (b) Explain the procedure for measurement of delay in floor planning.
   (c) What are the challenges in routing? Explain Global Routing.