MEC-902

RollNo. | | | | | | | | | | |

M.Tech.

(SEM I) ODD SEMESTER THEORY EXAMINATION, 2015-16

ANALOG CMOS DESIGN

Time: 3 Hours *Maximum Marks:100*

Note: *Attempt any five questions.*
All questions carry equal marks

1(a) Determine the small signal gain and the input common mode range (CMR) for the diff-amps shown in Fig 1. Estimate the slew-rate limitations in charging and discharging a 2pF capacitors tied to the outputs of the differential-amps as shown in figure 1

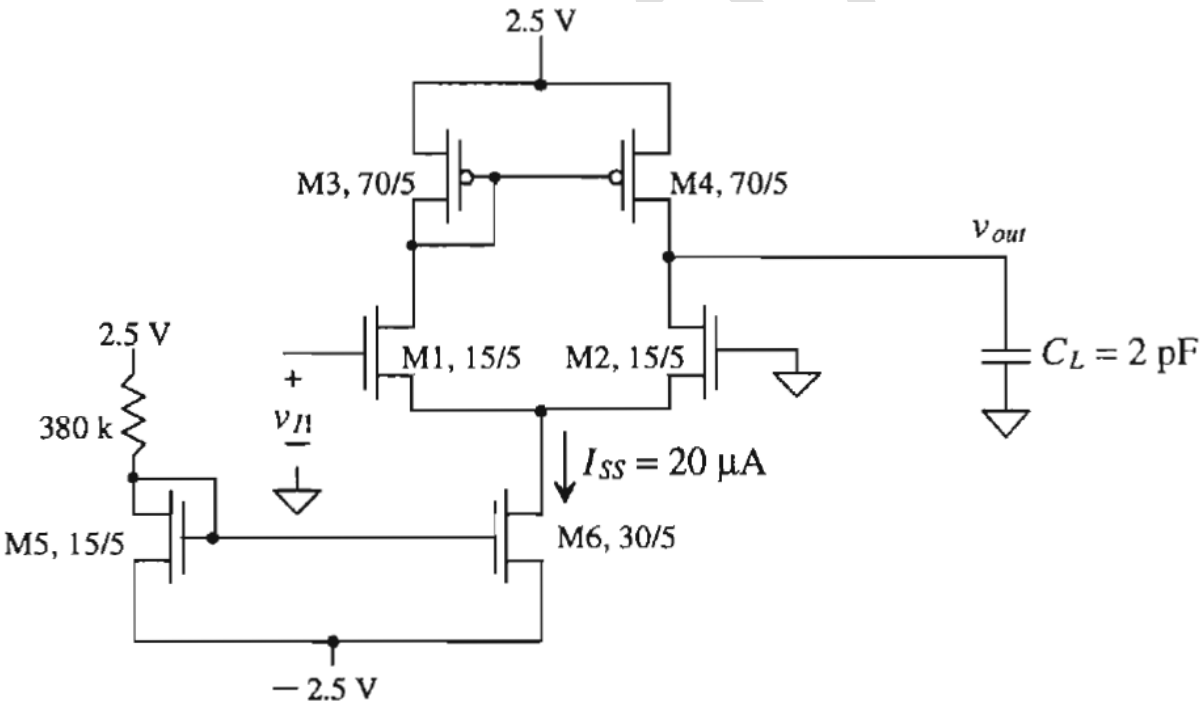

Figure 1

(b) Draw and analyze the cascode differential amplifier circuit using MOSFETs. What is the main drawback of this circuit?

2 (a) Develop a bandgap voltage reference circuit and determine the following:

(i) V_{ref}

(ii) The conditions under which the TC of the reference is zero.

(b) Design three current sources with values of 10, 20 and 50 μA using n- channel current sink of 10μA. Assume $V_{DD} = -V_{SS} = 2.5$ V, $V_{GS} = 1.2$ V and length of the devices = 5 μm, $V_{Thn} = 0.83$ V, $V_{Thp} = 0.91$V, $K_{pn} = 50$ μA /V^2 and $K_{pp} = 17$ μA /V^2.

3(a) Draw a CMOS Op-Amp circuit. Discuss design parameters with characteristic.

(b) Explain the two stage CMOS Op-Amp circuit analysis on the basic of the following design Parameter (i) Differential Amplifier Bias Current Iss (ii) Selection of the Second stage bias current.

4(a) Draw the CMOS configuration of Operational Transconductance Amplifier and discuss its advantages and limitations.

(b) Design a universal biquad g_m-C filter using two identical OTA and determine natural frequency and Q of the filter. Enlist the transfer function for each (i.e LP, HP, BP, BR) configuration.

5(a) A DAC has a full–scale voltage of 4.97 using a 5V reference, and its minimum output voltage is limited by the value of one LSB. Determine the resolution and dynamic range of the converter

(b) Design a 3-bit charge scaling DAC and find the value of the output voltage for $D_2D_1D_0$ =010. Assume that V_{REF} =5V and C=0.5pF

(c) Draw a block diagram of a Flash ADC and discuss its advantages and limitation

(d) Perform the operation of a 3-bit successive approximation ADC with $V_{REF} = 8$. Make a table that consists of $D_2D_1D_0$, B_2 B_1 B_0, V_{OUT} and the comparator output, which shows the binary search algorithm of the converter for $V_{IN} = 5.5$ V and 2.5 V.

6. Write short notes on the following

(a) Analog CMOS Multiplier

(b) CMOS Comparator

(c) Basic design of CMOS RF Circuits