Paper Code: MCA-215

Roll No. | | | | | | | | | | |

MCA
(SEM II) EVEN SEMESTER EXAMINATION, 2015-16
COMPUTER ORGANIZATION

[Time: 3 hrs.] **[Max. Marks: 100]**

Note-Attempt All questions .All questions carry equal marks.

1. Attempt any four of the following:- **[5x4=20]**

   (a) Show the block diagram of the hardware that implements the following register transfer statement: yT_2: R2 ← R1, R1← R.
   (b) Register A holds the 8-bit binary 11011001. Determine the B operand and the logic micro-operation to be performed in order to change the value in A to:
   (i) 01101101 (ii) 11111101
   (c) Explain the Booth's multiplication algorithm with flowchart. Also draw hardware logic diagram.
   (d) Draw the logic diagram using gates and flip-flops showing the circuit of one bus arbiter stage in the daisy-chain arbitration scheme.
   (e) Explain the different types of dynamic arbitration algorithms.
   (f) Show the step-by-step multiplication process using Booth's algorithm for (+15)X(+13). Assume 5-bit registers that hold signed numbers. The multiplicand is +15.

2. Attempt any four of the following:- **[5x4=20]**

   (a) Discuss the importance of control memory. Differentiate it from main memory.
   (b) Explain different fields of microinstruction with their use in micro-program execution.
   (c) Explain the role of micro-program sequencer in the control unit.
   (d) The control memory has 4096 words of 24 bits each.
      (i) How many bits are there in the control address register?
      (ii) What are the number of inputs in each multiplexer and how many multiplexers are needed?
   (e) Draw the 4-bit arithmetic circuit, which can execute arithmetic micro-operations.
   (f) Draw the logic circuit of bus system for four registers of four bits each. Explain its operation with function table.

3. Attempt any two of the following:- **[10x2=20]**

   (a) A bus organized CPU has 16 registers with 32 bits in each, an ALU, and a destination decoder.
      (i) How many multiplexers are there in the A bus, and what is the size of each multiplexer?
      (ii) How many selection inputs are needed for MUX A and MUX B?
      (iii) How many inputs and outputs are there in the decoder?
      (iv) How many inputs and outputs are there in the ALU for data, including input and output carriers?
      (v) *Formulate* the control word for the system assuming that the ALU has 35 operations.

   (b) A computer has 32-bit instruction and 12-bit addresses. If there are 250 two-address instructions, how many one-address instructions can be formulated?

   (c) Explain the Reduced Instruction Set Computer (RISC)? How it is different from Complex Instruction Set Computers (CISC)?

4. Attempt any two of the following:- **[10x2=20]**

   (a) What is the basic advantage of using interrupt-initiated data transfer over transfer under program control without an interrupt?

   (b) It is necessary to transfer 256 words from a magnetic disk to a memory section starting from address1230. The transfer is by means of DMA.

      (i) Give the initial values that the CPU must transfer to the DMA controller.

      (ii)Give the step-by-step account of the actions taken during the input of the first two words.

   (c) What is input-output interface? Describe different types of commands used.

5. Attempt any two of the following:- **[10x2=20]**

   (a) A computer uses RAM chips of 1024X1 capacities.

      (i) How many chips are needed, and how should their address lines be connected to provide a memory capacity of 1024 bytes?

      (ii) How many chips are needed to provide a memory capacity of 16K bytes? Explain in words how the chips are to be connected to the address bus?

   (b) The logical address space in the computer system consists of 128 segments. Each segment can have up to 32 pages of 4K words in each. Physical memory consists of 4K blocks4K words in each. Formulate the logical and physical address formats.

   (c) What is cache memory? Describe different types of mappings used in cache.