Paper Code: EEC-032	Roll No.									

B.Tech.
(SEM VIII) EVEN SEMESTER EXAMINATION, 2015-16
DIGITAL SYSTEM DESIGN USING VHDL

[Time: 3 hrs.] **[Max. Marks: 100]**

Note- Attempt All questions. All questions carry equal marks.

1. Attempt any four parts of the following:- **[5x4=20]**

   (a) Discuss how VHDL used to describe the behavior and structure of digital system.
   (b) Explain the VHDL function and procedure.
   (c) Using block diagram explain compilation, elaboration and simulation of VHDL codes
   (d) Write a VHDL description of an SR latch use two logic gates.
   (e) Explain different data types of VHDL codes.

2. Attempt any four parts of the following:- **[5x4=20]**

   (a) Explain Design validation of digital logic with block diagram.
   (b) Explain RTL design flow of VHDL codes.
   (c) Explain memory elements using procedural statements.
   (d) Write a VHDL code for a full subtractor using logic function.
   (e) Write a short note on synthesis of VHDL codes.

3. Attempt any two parts of the following:- **[10x2=20]**

   (a) Discuss about block statement and nested block statement with example.
   (b) What are the VHDL subprograms, explain each.
   (c) Explain in brief with codes (1) If statement (2) Case statement (3) Loop statement

4. Attempt any two parts of the following:- **[10x2=20]**

   (a) Discuss about inertial and Transport delay with logic diagram.
   (b) Explain concurrent and sequential assignment.
   (c) Explain in brief (1) Resolution function (2) Resolution Package (3) Bus kind resolved signal

5. Attempt any two parts of the following:- **[10x2=20]**

   (a) Write a VHDL code for shift register using process statement.
   (b) Explain data path and controller description.
   (c) Discuss about memory BIST architecture.