EEC-703

RollNo. | | | | | | | | | | |

B.Tech.

(SEM VII) ODD SEMESTER THEORY EXAMINATION, 2015-16

VLSI DESIGN

Time: 3 Hours *Maximum Marks:100*

Note: *Attempt all questions.*
All questions carry equal marks

Q.1. Write a short notes on any two of the following **10X2**

(a) VLSI design methodology (Y Chart) & MOS Scaling

(b) Write short notes on CAD Tools for VLSI Design & Enlist the classification of static CMOS digital logic families

(c) Discuss the layout design process of CMOS inverter. Draw a stick diagram of CMOS NOR gate.

Q.2. **Attempt any two parts of the following** **10X2**

(a) Consider a CMOS inverter circuits with the following parameters V_{DD} = 3.3V, V_{Ton} = 0.6V, V_{Top}= -0.7V, k_n = 200μA/V^2, k_p= 80μA/V^2, k_R = 2.5 Calculate the noise margin of the circuits.

(b) Consider a CMOS inverter, with the following device parameters, V_{DD} = 3.V, V_{Ton} = 0.6V, V_{Top} = -0.7V , $\mu_n C_{ox}$ = 60μA/V^2, $\mu_p C_{ox}$= 20μA/V^2, λ= 0. Determine the $\left(\frac{W}{L}\right)$ rations of the nMOS and the pMOS transistors such that the switching threshold is V_{th} = 1.5V.

(c) Design the circuit described by the Boolean function $Y = \overline{A.(B+C)(D+E)}$ using CMOS logic. Calculate the equivalent CMOS inverter circuit for simultaneous switching of all inputs assuming that $\left(\frac{W}{L}\right) = 5$ for pMOS transistor and $\left(\frac{W}{L}\right) = 2$ for all nMOS transistor.

Q.3. Attempt any two parts of the following **10X2**

(a) Discuss the classification of Dynamic CMOS logic families. Discuss the operation of pass transistor in dynamic logic circuit..

(b) Discuss the operation of five stage Ring Oscillator circuits & determine the oscillation frequency with PDP (R_n=8kΩ, R_p=24kΩ, C_{outn} =4.8fF, V_{DD} =5V).

(c) Estimate the intrinsic propagation delay t_{PHL}+t_{PLH} of a three-input NOR gate using minimum size transistor (R_n=8kΩ, R_p=24kΩ and C_{outn} =4.8fF).Estimate the circuit delay also when the gate is driving a load capacitance of 100fF.

Q.4. Attempt any two parts of the following **10X2**

(a) Discuss the Elmore Delay.In a CMOS inverter power supply V_{DD} =5V, determine the fall time, which is define as the time elapsed between the time point at which $V_{out}=V_{90\%}$ = 4.5V and the time point at which $V_{out}=V_{10\%}$ =0.5. The output load capacitance is 1pF. The nMOS transistor parameters are as follows: V_{Tn} = 1.0V, $\mu_n C_{ox}$ = 20μA/V^2, $\left(\frac{W}{L}\right)_n = 10$.

(b) Discuss the operation of single stage shift register circuits. Design a D flip-flop using TG CMOS logic circuits

(c) In a logic Design logic function is $Z = \overline{(A+B+C+D)(E+F+G)(H+I)}$ implemented with inputs (A,E,H) are high and other inputs are low. Draw a domino CMOS circuits diagram with implements Z.

Q. **5. Attempt any four parts of the following** **5X4**

(a) Define the terns Controllability and Observability.

(b) Explain the implementation of Built-In Self Test (BIST) design techniques for VLSI circuit testing.

(c) Write short notes on Adiabatic CMOS logic.

(d) Discuss the low power MTCMOS VLSI designs techniques.

(e) Draw and explain the operation of 6T CMOS SRAM cell circuit.

(f) Explain the overview of Power Consumption in CMOS logic circuits