Paper Code: EC 501	Roll No.									

B.Tech.
(SEM V) ODD SEMESTER EXAMINATION2015-16
INTEGRATED CIRCUITS

[Time: 3 hrs.] **[Max. Marks: 100]**

Note- ***Attempt All Questions. All Questions carry equal marks*:-**

1. **Attempt any two of the following:** **10x2=20**

a) Explain Widlar current source. **Figure 1**given below shows two circuits for generating a constant current I_O= 10μA which operate from a 10 V supply. Determine the values of the required resistor assuming that V_{BE} is 0.7 V at a current of 1 mA and neglecting of the effect of finite β.

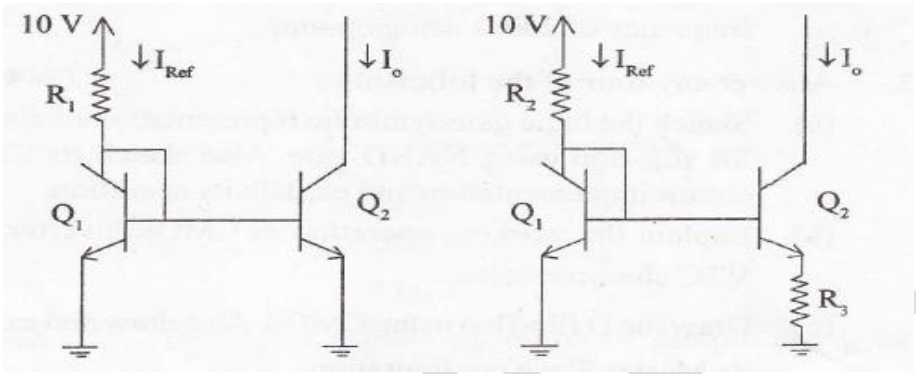

Fig. 1

b) A74l IC op-amp whose slew rate is 0.5 V/μs is used as an inverting amplifier with a gain of 50. The voltage gain Vs. frequency curve of 741IC is flat up to 20 kHz. What maximum peakto peak input signal can be applied without distorting the output?

c) How the short circuit protection is achieved in the output stage of 741 Op-Amp? Also, provide the DC analysis of Output Stage.

2. **Attempt any four of the following:** **5x4=20**

a) Draw and explain the most commonly used three Op-Amp Instrumentation Amplifier. Also, derive the expression of voltage gain.

b) Classify Active Filter and write its advantages with suitable examples.

c) Draw and explain V-I converter and derive its output equation.

d) Find Differential Gain of the circuit as shown in **figure 2.**

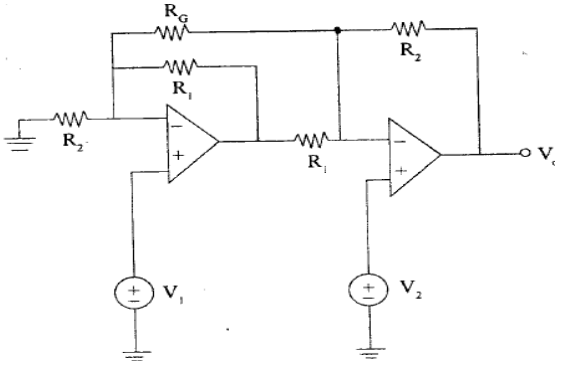

Fig. 2

e) Design a Second Order Low Pass Filter at a high cut off frequency of 2 kHz using op-amp.
f) Derive the expression for RC Phase Shift Oscillator.

3. Attempt any four of the following: 5x4=20

a) Explain the working operation of CMOS inverter with VTC characteristics.
b) Find truth table and CMOS realization of following gates.
(i) AND-OR-INVERT (AOI) => $F = \overline{AB + CD}$
(ii)OR-AND-INVERT (OAI) => $F = \overline{(A + B)(C + D)}$
c) Design CMOS logic circuit that realizes the function of three input parity checker specially the output is too high when an odd number (1 or 3) of the input is high.
d) Sketch the logic gate symbolic representation of clocked SR flip flop using NAND gate. Also sketch its CMOScircuit implementation and explain its operation.
e) Draw the D- Flip Flop using CMOS. Also draw and explain its Master Slave configuration.
f) Sketch the CMOS logic circuit realization of the following expression :
i. $Z = \overline{A(D + E) + BC}$
ii. $Z = \overline{(D + E + A)(B + C)}$

4. Attempt any two of the following: 10x2=20

a) Draw the circuit diagram of full wave precision rectifier and find its expression for output voltage for both positive and negative half cycle of input sinusoidal waveform.
b) Draw and explain operation of sample and hold circuit using op-amp.
c) Write short notes on any **two** of the following:
i. Analog multiplier.
ii. Log and Antilog amplifier.
iii. Zero crossing detector.

5. Attempt any two of the following: 10x2=20

a) Draw the functional block diagram of IC 555 and explain its working. Draw the circuit diagram of monostable multivibrator using 555 and find expression for quasi state period.
b) Draw the functional block diagram of PLL IC. Explain its working and deduce the expression for maximum frequency range of signal that can be locked.
c) Write short note on analog to digital converter.