EC-309 **Roll No.** | | | | | | | | | | |

B. Tech.

(SEM III) ODD SEMESTER EXAMINATION 2015-16

Digital Logic Design

[Time: 3Hrs.] **[Max Marks: 100]**

Note: *Attempt **All** Questions. All Questions carry equal marks*:-

1. Attempt any **four** parts: **(5 x 4 = 20)**
   (a) Perform the following operation:
      (i) $(11100111)_2 - (00110011)_2$ using 2's compliment methods.
      (ii) Perform the addition $(-32)_{10}$ and $(29)_{10}$ using binary signed 1's compliment notation for integers. You may assume that the maximum size of integers is of 8 bits including the sign bit.
      (iii) $(632)_{10}$ - $(129)_{10}$ using 10's compliment.
      (iv) Obtain the 84-2-1 code and 2421 code for $(259)_{10}$.
      (v) Obtain the Gray code and Octal code for $(39)_{10}$.
   (b) Implement full subtarctor employing two half subtractor and additional gates. Justify your answer.
   (c) Simplify the following function using Boolean algebra: $xy\bar{z} + \bar{x}yz + xyz + \bar{x}y\bar{z}$and implement by using NAND gate.
   (d) Minimize the following function by Tabular method F(w, x, y, z)=Σm(1, 4, 8, 9, 13, 14, 15) + d(2, 3, 11, 12)
   (e) Convert the following expression into sum of products and product of sums (i) $(AB + C)(B + \bar{C}D)$ (ii) $\bar{x} + x(x + \bar{y})(y + \bar{z})$
   (f) Design a combinational circuit that converts a 3-bit Gray code to a 3-bit binary number.
2. Attempt any f**our** parts: **(5 x 4 = 20)**
   (a) Implement full adder by using 3 to 8 line decoder and additional gates.
   (b) Implement the following function F(x, y, z)=Σm(0, 6)with the 2 level implementation (i) AND-NOR form (ii) Or-NAND form.
   (c) Design four-input priority encoder.
   (d) Implement the following function with a multiplexer using B, C, D variables to the select lines: F(A, B, C, D)=Σm(0, 1, 3, 4, 8, 9, 15).
   (e) Implement 4-bit magnitude comparator.
   (f) Design BCD adder and explain its operation.
3. Attempt any **two** parts: **(10 x 2 = 20)**
   (a) Write a short note on semiconductor memories. Distinguish between SRAM and DRAM. Draw and explain operation of SRAM cell.
   (b) Give the comparison of PROM, PLA and PAL. A combinational logic is defined by function:
   $F_1(A, B, C)=Σm(3, 5, 6, 7)$
   $F_2(A, B, C)=Σm(0, 2, 4, 7)$
   Implement the circuit with PLA having 3 inputs, 4 product terms and two outputs.

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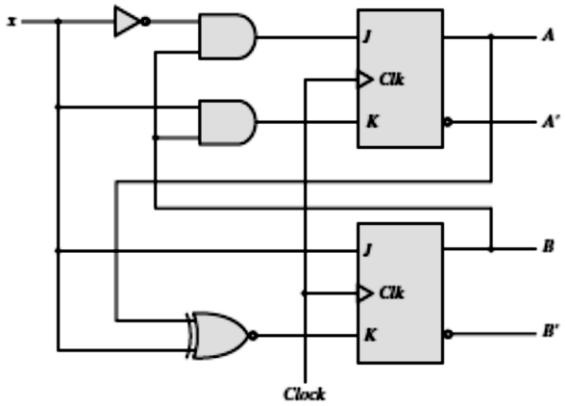
(c) Write a short note on Hamming code. If a 12 bit Hamming code word containing 8-bits of data and 4 parity bits is read from memory. What was the original 8-bit data word that was written into memory if the 12-bit word read out is as follows: 1011 1000 0110.

4. Attempt any **two** parts: **(10 x 2 = 20)**

(a) What do you mean by race-around condition and how can overcome with this problem? Draw logic diagram of master slave J-K flip-flop and write the characteristic table and characteristics equation for it.

(b) For the following logic diagram obtain input equation, state equation, output equation, state table and state diagram.



(c) What do you mean by counter? Design a counter that count in following sequence 0, 1, 2, 4, 5, 6, 0, 1, 2 … using T flip-flop.

5. Attempt any **two** parts: **(10 x 2 = 20)**

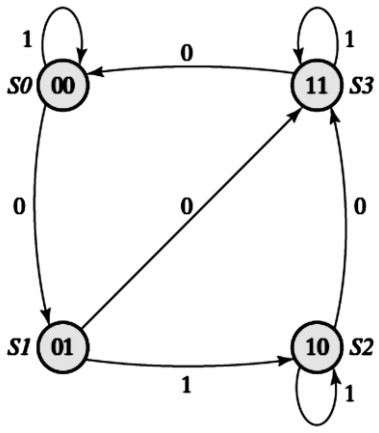
(a) An asynchronous sequential circuit has two internal states and one output. The exciation functions and output function of the circuit are as follows:

$$Y_1 = \bar{x}_1 x_2 + x_2 y_1$$
$$Y_2 = x_1 x y_2 + x_2$$

And output function

$$Z = x_1 + y_2$$

(b) Distinguish between synchronous and asynchronous sequential circuits. For the following state diagram obtain state table, excitation table and design circuit using J-K flip-flop.



(c) What do you mean by register? Explain the operation of universal shift register with neat logic diagram.