EC-302

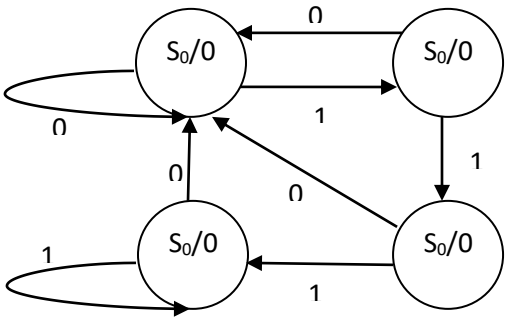
Roll No. | | | | | | | | | | |

B. Tech.
(SEM III) ODD SEMESTER EXAMINATION 2015-16
SWITCHING THEORY AND LOGIC DESIGN

[Time: 2Hrs.] [Max Marks: 50]

Note: *Attempt All Questions. All Questions carry equal marks*:-

1. Attempt any **two**: (7 x 2 = 14)
   (a) Perform the following operation:
      (i) $(10100111)_2 – (00110011)_2$ using 1's compliment methods.
      (ii) Perform the addition $(-32)_{10}$ and $(29)_{10}$ using binary signed 2's compliment notation for integers. You may assume that the maximum size of integers is of 8 bits including the sign bit.
      (iii) $(632)_{10}$ - $(129)_{10}$ using 9's compliment.
      (iv) Obtain the Ex-3 code and 2421 code for $(359)_{10}$.
      (v) Obtain the Gray code and Hex code for $(59)_{10}$.
      (vi) Implement XOR gate using minimum number of NAND gate.
      (vii) Write even parity and odd parity for the binary eight bit data $(10010011)_2$.
   (b) Minimize the following function by Tabular method and implement the result using NAND gate only: F(w, x, y, z)=Σm(1, 4, 8, 9, 13, 14, 15) + d(2, 3, 11, 12)
   (c) Design a combinational circuit that converts a 3-bit Gray code to a 3-bit binary number. Implement the circuit with (i) Ex-OR gate (ii) NAND gate only.
2. Attempt any **two**: (6 x 2 = 12)
   (a) Implement the following function F(x, y, z)=Σm(0, 6)with the 2 level implementation (i) AND-NOR form (ii) NAND-AND form (iii) Or-NAND form (iV) NOR-OR form.
   (b) Design four-input priority encoder.
   (c) (i) Implement the following function with a multiplexer using A, B, C variables to the select lines: F(A, B, C, D)=Σm(0, 1, 3, 4, 8, 9, 15).
   (ii)Implement 4-bit magnitude comparator.
3. Attempt any **two**: (6 x 2 = 12)
   (a) Differentiate between latches and flip-flops. What do you mean by race around condition and how can overcome with this problem? Explain briefly.
   (b) For the following state diagram obtain the state table, input equation, output equation and design the logic diagram using J-K flip-flop.



(c) An asynchronous sequential circuit has two internal states and one output. The exciation functions and output function of the circuit are as follows:

$$Y_1 = \bar{x}_1 x_2 + x_2 y_1$$
$$Y_2 = x_1 x y_2 + x_2$$

And output function

$$Z = x_1 + y_2$$

4. Attempt any **two**: (6 x 2 = 12)

(a) What do you mean by counter? Design a counter that count in following sequence 0, 1, 2, 4, 5, 6, 0, 1, 2 … using T flip-flop.

(b) What do you mean by register? How it can be classified? Write a short note on Johnson ring counter.

(c) Give the comparison of PROM, PLA and PAL. A combinational logic is defined by function:

$F_1(A, B, C)=\Sigma m(3, 5, 6, 7)$

$F_2(A, B, C)=\Sigma m(0, 2, 4, 7)$

Implement the circuit with PLA having 3 inputs, 4 product terms and two outputs.